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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,533	02/27/2002	Hiroshi Hashimoto	020244	6400

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EXAMINER	
LE, THAO X	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,533	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/29/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-10 and 12-40* is/are pending in the application.

4a) Of the above claim(s) *16-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-10,12-15 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0111695 to Kanamori in view of US 6294430 to Fastow et al.

Regarding claims 1, Kanamori discloses a semiconductor integrated circuit (IC) device in fig. 11A-11D, comprising: a substrate 101, a nonvolatile memory device formed in a memory cell region (with FG and CG) of substrate 101 and having a multilayer gate electrode G structure comprising a tunnel insulating film 111, fig. 5A, covering substrate 101 and floating gate electrode FG, fig. 10A, formed on the tunnel

insulating film 111 and having a side wall surfaces covered with a protection insulating film 115, fig. 8A formed of an oxide [0036]; a semiconductor device formed in a device region (MG), fig. 11D, of substrate 101, the semiconductor device comprising a gate insulating film 141 [0042] covering substrate 101 and gate electrode 114 [0042], formed on the gate insulating film 141; the gate insulating film 141 is interposed between substrate 101 and the gate electrode 114 have a uniform thickness at the region under the entire gate electrode 114, fig. 11D, wherein the protective insulating film 115 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure, fig. 8A; wherein the protective insulating film covers the multilayer gate electrode uniformly and sidewalls 117, fig. 9A, are formed over the protection insulating film 115, said side walls 117 covering the entire surface of the multilayer gate electrode structure, fig. 9A; and the multilayer gate electrode structure, including a control gate (CG) has a substantially uniform width, fig. 11A

But, Kanamori does not discloses wherein the bird's beak structure is formed at an interface of the tunnel insulating film and the floating gate electrode the bird's beak structure penetrating into the floating gate electrode along the interface from the sidewall faces of the floating gate electrode 10a semiconductor device

However, Fastow discloses a semiconductor device in fig. 3G comprising a bird's beak (334), a tunnel oxide, a floating gate 308, a ONO dielectric 310, a control gate 312 and a protective insulating film 314/332 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure; and

wherein the protective insulating film covers the multilayer gate electrode uniformly. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the protective insulating film 314/332 teaching of Fastow with Kanamori's device, because it would have reduces the number of oxides traps in the bird's beak region of the tunnel oxide thus improving the reliability of the floating gate memory device as taught by Fastow in col. 1 lines 10-15.

Regarding claims 2-3, 12, Kanamori discloses the IC device wherein the multiplayer gate electrode structure further comprises an insulating film 113 [0036], formed on the floating gate electrode FG, and a control gate electrode CG, formed on the insulating film 1113, wherein each of the gate electrode 114 and control gate electrode CG comprises doped polysilicon [0036].

Regarding claims 4 and 10, Kanamori does not disclose the IC device wherein the oxide film connects the bird's beak structure.

However, Fastow discloses in fig. 3G the IC device wherein the oxide film connects314 the bird's beak structure 334 for the same reason as discussed in claim 1.

Regarding claims 7 and 14, Kanamori discloses the IC device having the tunnel oxide 111.

Regarding claim 9, Kanamori discloses a semiconductor integrated circuit device in fig. 11A-11D comprising: a substrate 101, a nonvolatile memory device formed in a memory cell region (FG, CG) of said substrate 101, the nonvolatile memory device

comprising: a first active region S covered with a tunnel insulating film 111, formed next to the first active region S and covered with an insulating film 113, a control gate CG formed of an embedded diffusion region formed in the first active region; a first gate electrode FG extending on the tunnel insulating film 111 in the first active region S and forming a bridge between the first and second active regions S/D to be capacitive-coupled via the insulating film 113 to the embedded diffusion region in the first active region S, the first gate electrode FG having sidewall faces thereof covered with a protection insulating film 115 formed of a oxide film; and a diffusion region formed on each of sides of the first gate electrode FG in the first active region; and a semiconductor device formed in a device region (MG) of substrate 101, the semiconductor device comprising a gate insulating film 141 covering substrate 101 and a second gate electrode 114, fig. 9D, formed on the gate insulating film 141, fig. 8D, and the second gate electrode 114 to have a uniform thickness at the region under the entire gate electrode 114, fig. 11D; wherein the protective insulating film 115 covers a top surface of the first gate electrode FG electrode uniformly and sidewalls 117, fig. 9A, are formed over the protection insulating film 115, said side walls 117 covering the entire surface of the first gate electrode FG, fig. 9A; and the first gate electrode FG has a substantially uniform width, fig. 11A.

But, Kanamori does not discloses wherein the bird's beak structure is formed at an interface of the tunnel insulating film and the floating gate electrode the bird's beak structure penetrating into the floating gate electrode along the

interface from the sidewall faces of the floating gate electrode 10a semiconductor device

However, Fastow discloses a semiconductor device in fig. 3G comprising a first active region n and n+ (double diffused regions), fig. 1 and fig. 3G, a bird's beak (334), a tunnel oxide, a floating gate 308, a ONO dielectric 310, a control gate 312 and a protective insulating film 314/332 continuously covers sidewall faces and a top surface of the multilayer gate electrode structure; and wherein the protective insulating film covers the multilayer gate electrode uniformly. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the double diffused regions and protective insulating film 314/332 teaching of Fastow with Kanamori's device, because it would have created an EEPROM device reducing the number of oxides traps in the bird's beak region of the tunnel oxide thus improving the reliability of the floating gate memory device as taught by Fastow in col. 1 lines 10-15.

Regarding claim 40, as discussed in the above claims 1-4, and 12, the combination of Kanamori and Fastow disclose all the limitations of claim 40.

4. Claims 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0111695 to Kanamori et al. and US 6294430 to Fastow et al. as applied to claims 1 and 9 above and further in view of US 6406959 to Prall et all.

Regarding claims 6, 13, Kanamori does not expressly disclose the semiconductor IC device wherein a SOI substrate is employed as substrate.

However, Prall reference discloses a flash memory device wherein the substrate 11 can be either silicon or SOI, column 4 line 15. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the silicon substrate of Kanamori with either Si or SOI substrate teaching of Prall, because such substrate substitution would have been considered a mere substitution of art-recognized equivalent values.

5. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2003/0111695 to Kanamori et al and US 6294430 to Fastow et al. as applied to claims 1 and 9 above and further in view of Applicant Admitted Prior Art (APA)

Regarding to claims 8 and 15, Kanamori does not discloses the tunnel insulating film is a nitride oxide film.

However, APA discloses the IC device having the tunnel oxide 12, spec. page 2 or nitride, page 4. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the tunnel insulating material teaching of APA in the Kanamori's device, because such material substitution would have been considered a mere substitution of art-recognized equivalent values.

Response to Arguments

6. Applicant's arguments with respect to claims 1-4, 6-10, 12-15 and 40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

04 Mar. 2007

THAO X. LE
PRIMARY PATENT EXAMINER